AMENDMENTS TO THE CLAIMS

Please **CANCEL** claim 44 without prejudice or disclaimer.

Please **AMEND** claims 10 and 40, 42, 43, 45 and 46 as shown below.

Please **ADD** claims 47-55 as shown below.

The following is a complete list of all claims in this application.

1. (Withdrawn) A method for manufacturing a contact structure of a wire, comprising steps of:

forming a wire made of a metal;

depositing an inorganic insulating layer covering the wire;

executing a thermal treatment process;

patterning the inorganic insulating layer to form a contact hole exposing a reaction layer on the wire; and

forming a conductive layer electrically connected to the wire.

2. (Withdrawn) The method of claim 1, wherein the wire is made of a conductive material including aluminum-based material.

3. (Withdrawn) The method of claim 1, wherein the inorganic insulating layer is made of silicon-nitride.

4. (Withdrawn) The method of claim 1, wherein the inorganic insulating layer is deposited at a temperature range of 250-400℃.

5. (Withdrawn) The method of claim 1, wherein the conductive layer is made of a transparent conductive material.

6. (Withdrawn) The method of claim 5, wherein the conductive layer is made of indium zinc oxide.

7. (Withdrawn) The method of claim 6, wherein the indium zinc oxide is formed at a temperature range of less than 250℃.

8. (Withdrawn) The method of claim 1, wherein the thermal treatment process is executed through an annealing step.

9. (Withdrawn) The method of claim 8, wherein the annealing step is executed at a temperature range of 280-400℃.

10. (Currently Amended) A contact structure of a wire, comprising:

a wire ~~including~~ formed of aluminum ~~a conductive material made of an aluminum-based material~~;

an inorganic insulating layer covering the wire and having a contact hole exposing the wire; and

a conductive layer ~~made~~ formed of indium zinc oxide (IZO), ~~formed~~ on the insulating layer and connected to and directly contacting the wire through the contact hole.

11. (Previously Presented) The contact structure of claim 10, wherein the contact hole has a shape including rounds or corner, and size of the contact hole is greater than 4 μm * 4 μm.

12. (Original) The contact structure of claim 10, wherein the inorganic insulating layer is made of silicon-nitride.

13. (Original) The contact structure of claim 10, wherein the wire has a flat surface.

14. (Withdrawn) A manufacturing method of a thin film transistor array panel, comprising steps of:

forming a gate wire;

forming a data wire;

forming a semiconductor layer;

forming an insulating layer covering the gate wire, the data wire or the semiconductor layer;

executing a thermal treatment process;

forming a contact hole exposing the gate wire or the data wire by patterning the insulating layer; and

forming a conductive layer electrically connected to the gate wire or the data wire through the contact hole.

15. (Withdrawn) The method of claim 14, wherein the gate wire and the data wire include a conductive material of aluminum-based material.

16. (Withdrawn)The method of claim 14, wherein the insulating layer is made of silicon-nitride.

17. (Withdrawn)The method of claim 14, wherein the insulating layer is deposited at a temperature range of 250-400℃.

18. (Withdrawn)The method of claim 14, wherein the conductive layer is made of indium zinc oxide.

19. (Withdrawn)The method of claim 18, wherein the indium zinc oxide is formed at a temperature range of less than 250 ℃.

20. (Withdrawn)The method of claim 14, wherein the thermal treatment process is executed through an annealing step.

21. (Withdrawn)The method of claim 20, wherein the annealing step is executed at a temperature range of 250-400℃.

22. (Withdrawn)A manufacturing method of a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line, and a gate electrode connected to the gate line by depositing and patterning a first conductive material on an insulating substrate;

depositing a gate insulating layer;

forming a semiconductor layer;

forming a data wire including a data line intersecting the gate line, a source electrode connected to the data line and adjacent to the gate electrode and a drain electrode opposite to the source electrode with respect to the gate electrode by depositing and patterning a second conductive material;

depositing a passivation layer;

executing a thermal treatment process;

patterning the passivation layer to form a first contact hole exposing the drain electrode; and

forming a pixel electrode electrically connected to the drain electrode through the first contact hole on the passivation layer.

23. (Withdrawn)The method of claim 22, wherein the first and the second conductive material include a metal of aluminum-based material.

24. (Withdrawn) The method of claim 22, wherein the insulating layer and the passivation layer are deposited at a temperature range of 250-400℃.

25. (Withdrawn) The method of claim 22, wherein the insulating layer and the passivation layer are made of silicon-nitride.

26. (Withdrawn) The method of claim 22, wherein the pixel electrode is made of a transparent conductive material.

27. (Withdrawn) The method of claim 26, wherein the pixel electrode is made of indium zinc oxide.

28. (Withdrawn) The method of claim 27, wherein the indium zinc oxide is formed at a temperature range of less than 250℃.

29. (Withdrawn) The method of claim 22, wherein the thermal treatment is executed through an annealing step.

30. (Withdrawn) The method of claim 29, wherein the annealing step is executed at a temperature range of 250-400℃.

31. (Withdrawn) The method of claim 22, wherein the gate wire further includes a gate pad that is connected to the gate line and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to the data line and receives a signal from an external circuit, and the passivation layer and the gate insulating layer have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad, and

further comprising the step of forming a redundant gate pad and a redundant data pad that are made of the same layer as the pixel electrode and respectively electrically connected to the gate pad and the data pad through the second and the third contact holes.

32. (Withdrawn) The method of claim 22, wherein the data wire and the semiconductor layer are together formed by a photolithography process using a photoresist pattern having different thicknesses depending the positions.

33. (Withdrawn) The method of claim 32, wherein the photoresist pattern has a first portion having a first thickness, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

34. (Withdrawn) The method of claim 33, wherein a mask used for forming the photoresist pattern has a first, a second, and a third part, a transmittance of the third part is higher than the first and the second parts, a transmittance of the first part is higher than the second part.

35. (Withdrawn) The method of claim 34, wherein the first and the second portion of the photoresist pattern are respectively aligned on portion between the source electrode and the drain electrode, and the data wire.

36. (Withdrawn) The method of claim 35, wherein the first part of the mask includes a partially transparent layer, or a slit pattern smaller than the resolution of the exposure used in the exposing step, to regulate the transmittance of the first part.

37. (Withdrawn) The method of claim 36, wherein the thickness of the first portion is less than a half of the thickness of the second portion.

38. (Withdrawn) The method of claim 22, further comprising step of:

depositing an ohmic contact layer between the data wire and the semiconductor layer.

39. (Withdrawn) The method of claim 38, wherein the data wire, the ohmic contact layer, and the semiconductor layer are formed in the same photolithography process.

40. (Currently Amended) A thin film transistor (TFT) array panel, comprising:

a gate wire ~~including a first conductive layer~~ formed on an insulating substrate;

a gate insulating layer covering the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire ~~including a second conductive layer~~ formed of aluminum on the gate insulating layer and the semiconductor layer;

a passivation layer covering the data wire; and

a transparent conductive layer formed of indium zinc oxide (IZO) ~~pattern directly contacting with and connected to the gate wire through a first contact hole of the gate insulating layer or~~ directly contacting ~~with~~ and connected to the data wire through the passivation layer~~,~~

~~wherein the first conductive layer and the second conductive layer includes aluminum metal containing an aluminum-based material~~.

41. (Cancelled)

42. (Currently Amended) The ~~thin film transistor~~ TFT array panel of claim 40, wherein the data wire has a flat surface ~~of the metal containing the aluminum-based material is flat~~.

43. (Currently Amended) The ~~thin film transistor~~ TFT array panel of claim 40, wherein the insulating layer and the passivation layer are made of silicon-nitride.

44. (Cancelled)

45. (Currently Amended) The ~~thin film transistor~~ TFT array panel of claim 40, wherein the gate wire includes a gate line, a gate electrode connected to the gate line, and a gate pad ~~which is~~ connected to the gate line ~~and receives a signal from an external circuit~~, and

the data wire includes a data line, a source electrode connected to the data line, a drain electrode separated from the source electrode and opposite to the source electrode with respect to

the gate electrode, and a data pad ~~that is~~ connected to the data line ~~and receives a signal from an external circuit~~.

46. (Currently Amended) The ~~thin film transistor~~ TFT array panel of claim 45, wherein the passivation layer further comprises a second contact hole exposing the data pad and a third contact hole exposing the gate pad along with the gate insulating layer, the first to the third contact holes have a shape including rounds or corner, and a size of the first to the third contact holes are greater than 4 μm * 4 μm.

47. (New) The TFT array panel of claim 40, wherein the gate wire is formed of aluminum.

48. (New) The TFT array panel of claim 47, wherein the transparent conductive layer comprises:

a first pattern directly contacting and connected to the gate wire through the gate insulating layer; and

a second pattern directly contacting and connected to the data wire through the passivation layer.

49. (New) A thin film transistor (TFT) array panel , comprising:

a substrate;

a gate wire formed of aluminum on the substrate and comprising a gate pad and a gate line extended from the gate pad;

a gate insulating layer covering the gate wire;

a data wire formed of aluminum on the gate insulating layer and comprising a data line, a source electrode connected to the data line and a drain electrode separated from the source electrode;

a passivation layer covering the data wire; and

a transparent conductive layer formed of indium zinc oxide (IZO) having a first pattern directly contacting and connected to the gate pad through the gate insulating layer and a second pattern directly contacting and connected to the drain electrode through the passivation layer.

50. (New) The TFT array panel of claim 49, wherein the data wire is formed by annealing.

51. (New) The TFT array panel of claim 50, wherein the gate wire is formed by annealing.

52. (New) The TFT array panel of claim 49, wherein the passivation layer is formed of silicon nitride.

53. (New) The TFT array panel of claim 49, wherein the transparent conductive layer formed of IZO is formed from an IZO target including In_2O_3 and ZnO with a Zn content ranged between 15% to 20%.

54. (New) The contact structure of claim 10, wherein the conductive layer formed of IZO is formed from an IZO target including In_2O_3 and ZnO with a Zn content ranged between 15% to 20%.

55. (New) The TFT array panel of claim 40, wherein the transparent conductive layer formed of IZO is formed from an IZO target including In_2O_3 and ZnO with a Zn content ranged between 15% to 20%.